Radiation Hardened Ultra High Frequency NPN/PNP Transistor Arrays

ISL73096RH, ISL73127RH, ISL73128RH, ISL73096EH, ISL73127EH, ISL73128EH

The ISL73096, ISL73127 and ISL73128 are radiation hardened bipolar transistor arrays. The ISL73096 consists of three NPN transistors and two PNP transistors on a common substrate. The ISL73127 consists of five NPN transistors on a common substrate. The ISL73128 consists of five PNP transistors on a common substrate.

The ISL73096EH, ISL73127EH and ISL73128EH devices encompass all of the production testing of the ISL73096RH, ISL73127RH and ISL73128RH devices and additionally are tested in the Intersil Enhanced Low Dose Rate Sensitivity (ELDERS) product manufacturing flow.

One of our bonded wafer, dielectrically isolated fabrication processes provides an immunity to single event latch-up and the capability of highly reliable performance in a radiation environment.

The high gain-bandwidth product and low noise figure of these transistors make them ideal for use in high frequency amplifier and mixer applications. Monolithic construction of the NPN and PNP transistors provides the closest electrical and thermal matching possible. Access is provided to each terminal of the transistors for maximum application flexibility.

Related Literature

- AN1503. Amplifier Design Using ISL73096RH, ISL73127RH, ISL73128RH Transistor Arrays
- TID REPORT for the Radiation Hardened UHF NPN/PNP transistor array

Features

- Electrically screened to SMD # 5962-07218
- QML qualified per MIL-PRF-38535 requirements
- Radiation tolerance
  - High dose rate (50-300rad(Si)/s). . . . . 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . . 50krad(Si)*
  - SEL immune . . . . . Bonded wafer dielectric isolation
- NPN gain bandwidth product (F_T) . . . . . 8GHz (typ)
- NPN current gain (h_{FE}) . . . . . 130 (typ)
- NPN early voltage (V_A). . . . . 50V (typ)
- PNP gain bandwidth product (F_T). . . . . 5.5GHz (typ)
- PNP current gain (h_{FE}). . . . . 60 (typ)
- PNP early voltage (V_A) . . . . . 20V (typ)
- Noise figure (50Ω) at 1GHz. . . . . 3.5dB (typ)
- Collector-to-collector leakage . . . . . <1pA (typ)
- Complete isolation between transistors

* Limit established by characterization.

Applications

- High frequency amplifiers and mixers
- High frequency converters
- Synchronous detector

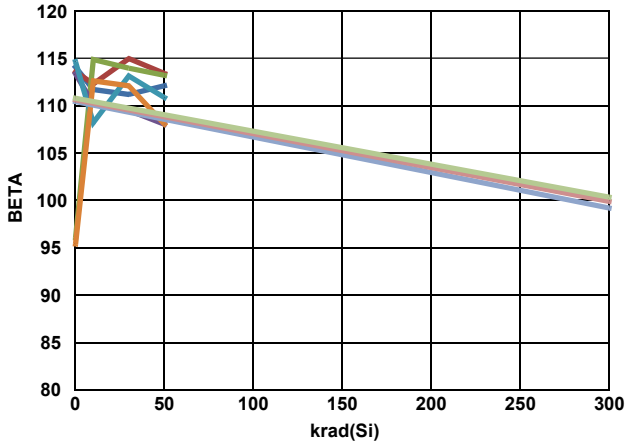


FIGURE 1. NPN BETA OVER TOTAL IONIZING DOSE (TID) FOR LOW DOSE RATE (LDR) TO 50krads(Si) AND HIGH DOSE RATE (HDR) TO 300krads(Si)

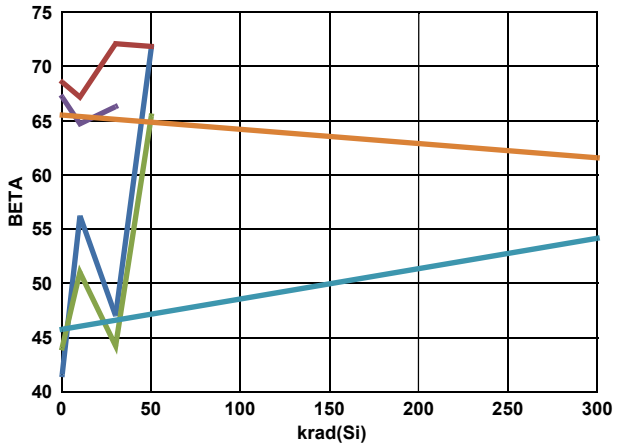


FIGURE 2. PNP BETA OVER TOTAL IONIZING DOSE (TID) FOR LOW DOSE RATE (LDR) TO 50krads(Si) AND HIGH DOSE RATE (HDR) TO 300krads(Si)

Typical Applications

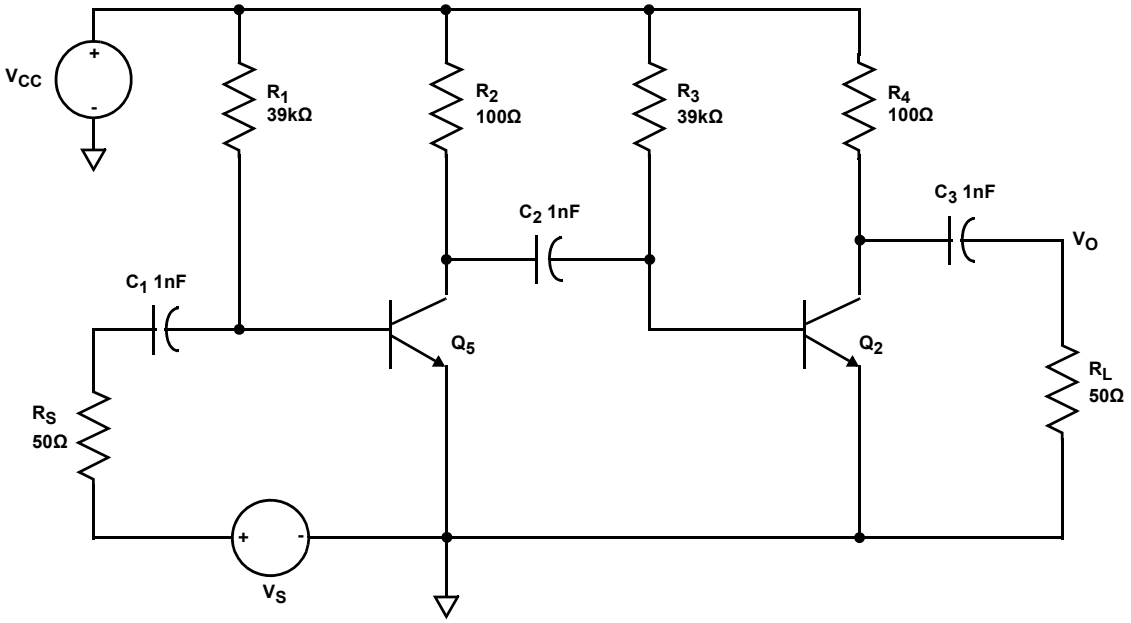


FIGURE 3. HIGH-GAIN, LOW-NOISE AMPLIFIER MADE FROM ISL73127

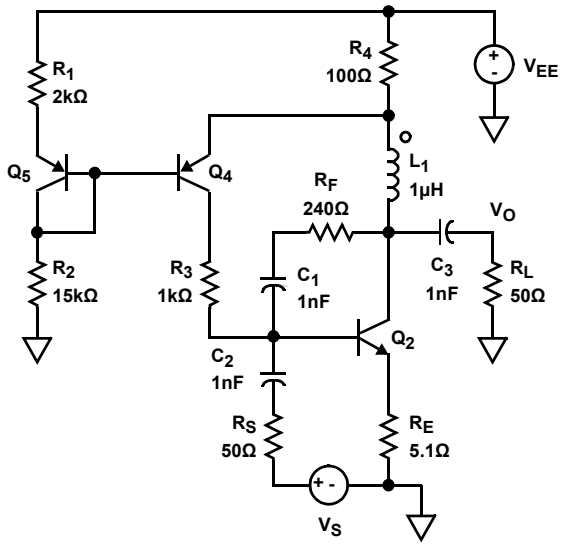


FIGURE 4. WIDEBAND AMPLIFIER MADE FROM ISL73096

Ordering Information

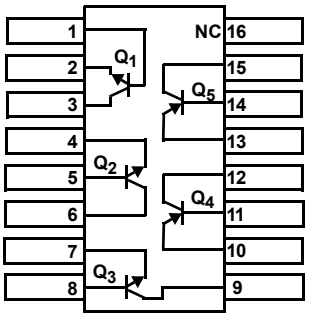
ORDERING SMD NUMBER	PART NUMBER (Notes 1, 2)	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
5962F0721804VXC	ISL73096EHVF	-55 to +125	16 Ld FLATPACK	K16.A
5962F0721801VXC	ISL73096RHVF	-55 to +125	16 Ld FLATPACK	K16.A
5962F0721801V9A	ISL73096RHVX	-55 to +125	DIE	
5962F0721804V9A	ISL73096EHVX	-55 to +125	DIE	
5962F0721805VXC	ISL73127EHVF	-55 to +125	16 Ld FLATPACK	K16.A
5962F0721802VXC	ISL73127RHVF	-55 to +125	16 Ld FLATPACK	K16.A
5962F0721802V9A	ISL73127RHVX	-55 to +125	DIE	
5962F0721805V9A	ISL73127EHVX	-55 to +125	DIE	
5962F0721806VXC	ISL73128EHVF	-55 to +125	16 Ld FLATPACK	K16.A
5962F0721803VXC	ISL73128RHVF	-55 to +125	16 Ld FLATPACK	K16.A
5962F0721803V9A	ISL73128RHVX	-55 to +125	DIE	
5962F0721806V9A	ISL73128EHVX	-55 to +125	DIE	
ISL73096RHF/PROTO	ISL73096RHF/PROTO	-55 to +125	16 Ld FLATPACK	K16.A
ISL73096RHX/SAMPLE	ISL73096RHX/SAMPLE	-55 to +125	DIE	
ISL73127RHF/PROTO	ISL73127RHF/PROTO	-55 to +125	16 Ld FLATPACK	K16.A
ISL73127RHX/SAMPLE	ISL73127RHX/SAMPLE	-55 to +125	DIE	
ISL73128RHF/PROTO	ISL73128RHF/PROTO	-55 to +125	16 Ld FLATPACK	K16.A
ISL73128RHX/SAMPLE	ISL73128RHX/SAMPLE	-55 to +125	DIE	

NOTES:

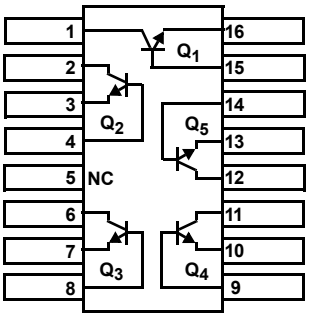
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the Ordering Information table must be used when ordering.

Pin Configurations

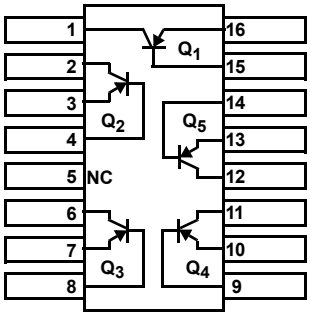
ISL73096RH, ISL73096EH
(16 LD FLATPACK) CDFP4-F16
TOP VIEW



ISL73127RH, ISL73127EH
(16 LD FLATPACK) CDFP4-F16
TOP VIEW



ISL73128RH, ISL73128EH
(16 LD FLATPACK) CDFP4-F16
TOP VIEW



Pin Descriptions

PIN #	PIN NAME/DESCRIPTION ISL73096RH, ISL73096EH	PIN NAME/DESCRIPTION ISL73127RH/ISL73128RH ISL73127EH/ISL73128EH
1	Q1 BASE	Q1 COLLECTOR
2	Q1 EMITTER	Q2 COLLECTOR
3	Q1 COLLECTOR	Q2 EMITTER
4	Q2 EMITTER	Q2 BASE
5	Q2 BASE	NC (No internal Connection)
6	Q2 COLLECTOR	Q3 COLLECTOR
7	Q3 EMITTER	Q3 EMITTER
8	Q3 BASE	Q3 BASE
9	Q3 COLLECTOR	Q4 BASE
10	Q4 EMITTER	Q4 EMITTER
11	Q4 BASE	Q4 COLLECTOR
12	Q4 COLLECTOR	Q5 COLLECTOR
13	Q5 EMITTER	Q5 EMITTER
14	Q5 BASE	Q5 BASE
15	Q5 COLLECTOR	Q1 BASE
16	NC (No internal Connection)	Q1 EMITTER

Absolute Maximum Ratings

Collector to Emitter Voltage (Open Base)
- ISL73096, ISL73127 (NPN Characteristics) . . . . . +8V
- ISL73096, ISL73128 (PNP Characteristics) . . . . . -8V

Collector to Base Voltage (Open Emitter)
- ISL73096, ISL73127 (NPN Characteristics) . . . . . +12V
- ISL73096, ISL73128 (PNP Characteristics) . . . . . -10V

Emitter to Base Voltage (Reverse Bias)
- ISL73096, ISL73127 (NPN Characteristics) . . . . . +5.5V
- ISL73096, ISL73128 (PNP Characteristics) . . . . . -4.5V

Collector Current at 100% Duty Cycle, at T_J +175°C 11.3mA
Power Dissipation (Pd), at T_A +25°C 1.25W
Power Dissipation (Pd), at T_A +125°C 0.41W

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld FLATPACK Package(Notes 3, 4) . . .	120	28

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +175°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the package underside.

Electrical Specifications

T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; across a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300 rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure a low dose rate of <10mrad(Si)/s at +25°C.**

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
NPN PARAMETER						
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100µA, I_E = 0	**12**			V
$V_{(BR)CEO}$	Collector to Emitter Breakdown Voltage	I_C = 100µA, I_B = 0	**8**			V
$V_{(BR)CES}$	Collector to Emitter Breakdown Voltage	I_C = 100µA, base shorted to emitter	**10**			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 10µA, I_C = 0	**5.5**			V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = 10mA, I_B = 1mA			**0.5**	V
V_{BE}	Base to Emitter Voltage	I_C = 10mA			0.95	V
					1.05	V
h_{FE}	DC Forward Current Transfer Ratio	I_C = 10mA, V_{CE} = 2V	80			
			40			
V_A	Early Voltage	I_C = 1mA, V_{CE} = 3.5V	**20**			V
PNP PARAMETER						
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = -100µA, I_E = 0	**10**			V
$V_{(BR)CEO}$	Collector to Emitter Breakdown Voltage	I_C = -100µA, I_B = 0	**8**			V
$V_{(BR)CES}$	Collector to Emitter Breakdown Voltage	I_C = -100µA, base shorted to emitter	**10**			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = -10µA, I_C = 0	**4.5**			V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = -10mA, I_B = -1mA			**0.5**	V
V_{BE}	Base to Emitter Voltage	I_C = -10mA			0.95	V
					1.05	V
h_{FE}	DC Forward Current Transfer Ratio	I_C = -10mA, V_{CE} = -2V	40			
			20			
V_A	Early Voltage	I_C = -1mA, V_{CE} = -3.5V	**10**			V

NOTE:

5. Compliance to data sheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

+25°C unless otherwise specified.

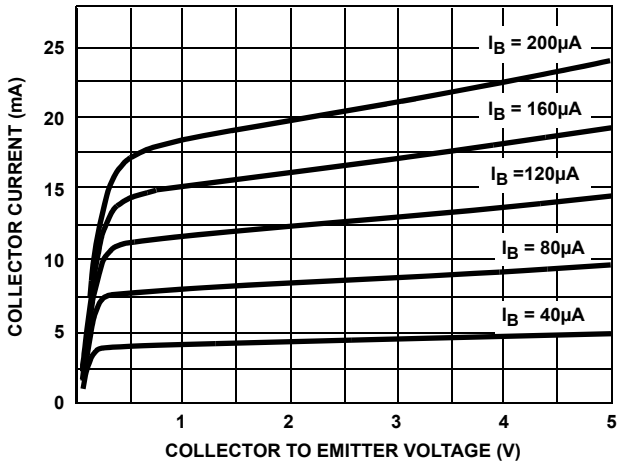


FIGURE 5. NPN COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE

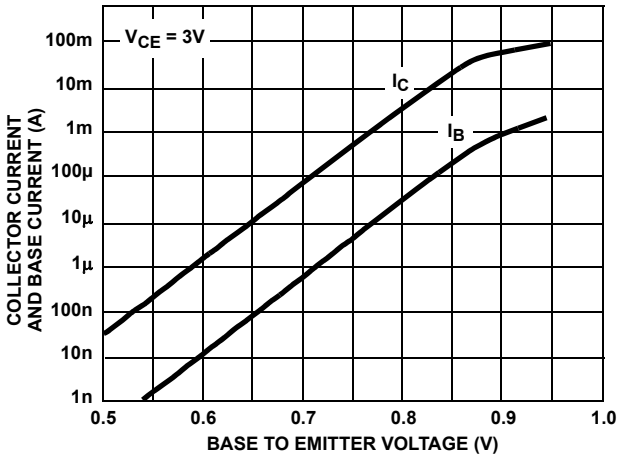


FIGURE 6. NPN COLLECTOR CURRENT AND BASE CURRENT vs BASE TO EMITTER VOLTAGE

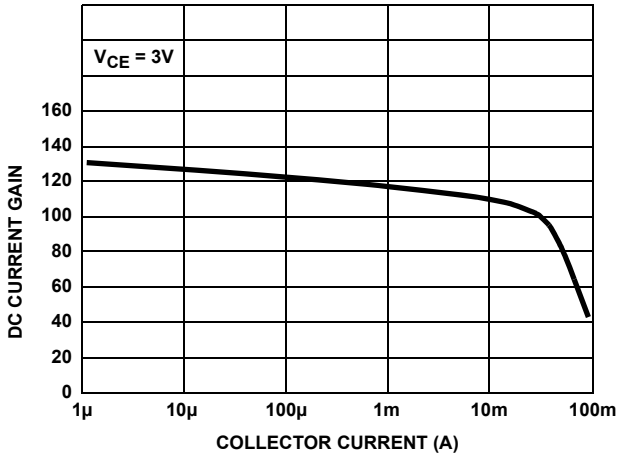


FIGURE 7. NPN DC CURRENT GAIN vs COLLECTOR CURRENT

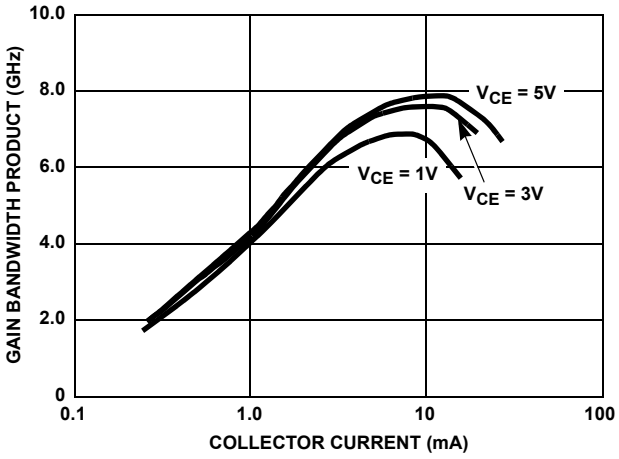


FIGURE 8. NPN GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT

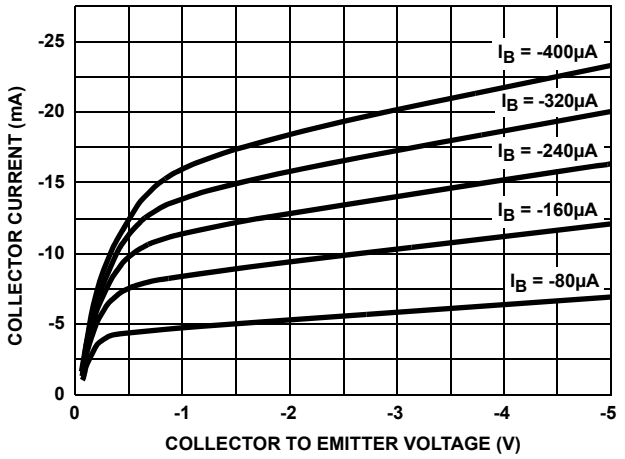


FIGURE 9. PNP COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE

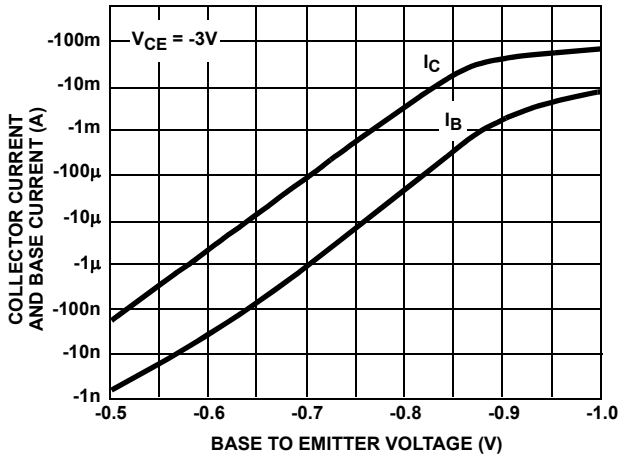


FIGURE 10. PNP COLLECTOR CURRENT AND BASE CURRENT vs BASE TO EMITTER VOLTAGE

Typical Performance Curves

+25°C unless otherwise specified. **(Continued)**

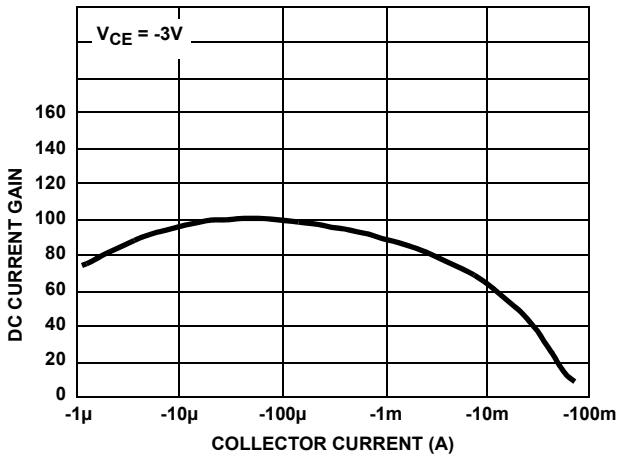


FIGURE 11. PNP DC CURRENT GAIN vs COLLECTOR CURRENT

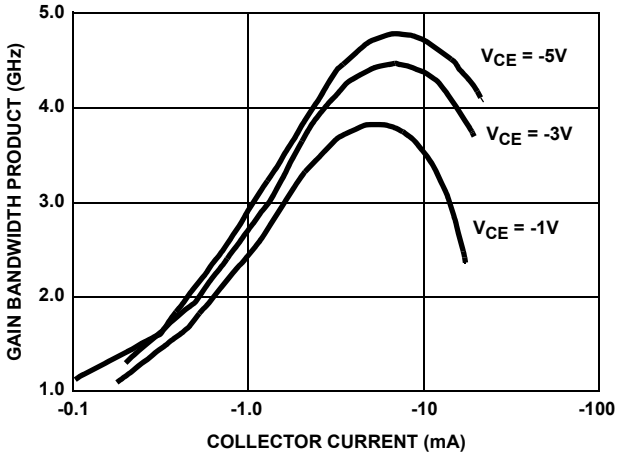


FIGURE 12. PNP GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT

Die Characteristics

DIE DIMENSIONS:

52.8 mils x 52.0 mils x 14 mils ±1 mil
1340µm x 1320µm x 355.6µm ±25.4µm

INTERFACE MATERIALS:

Glassivation:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

Top Metallization:

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8kÅ ±0.5kÅ
Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

Substrate:

UHF-1X Bonded Wafer, DI

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Floating

ADDITIONAL INFORMATION:

Worst Case Current Density:

$3.04 \times 10^5 A/cm^2$

Transistor Count:

5

Metallization Mask Layout

FIGURE 13. ISL73096RH, ISL73096EH

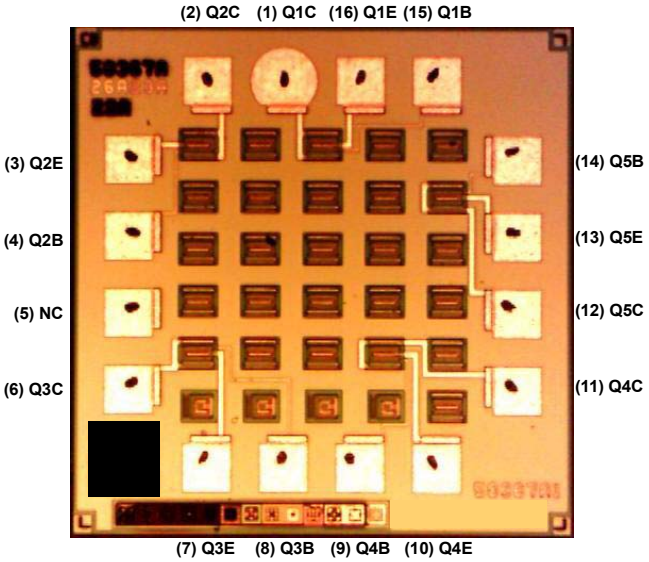


FIGURE 14. ISL73127RH, ISL73127EH

Metallization Mask Layout (Continued)

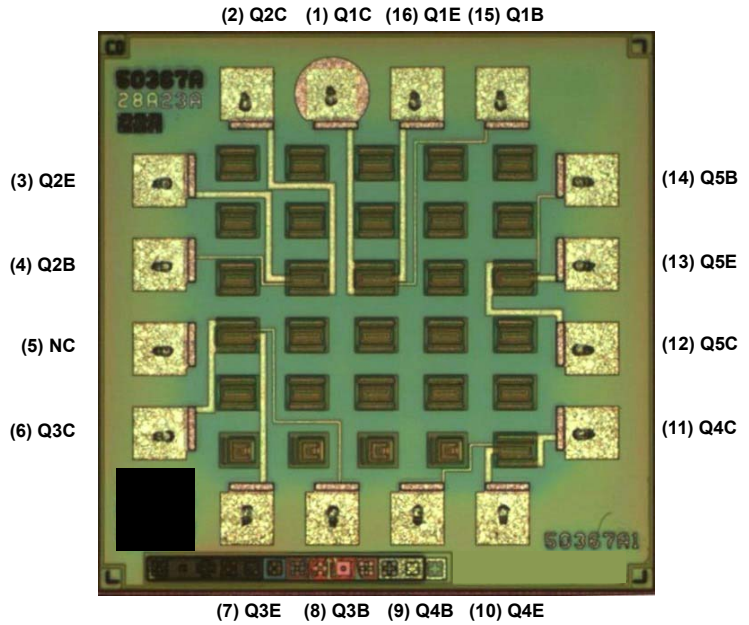


FIGURE 15. ISL73128RH, ISL73128EH

TABLE 1. DIE LAYOUT X-Y COORDINATES

BOND PAD NUMBER	X (MILS)	Y (MILS)	dX (MILS)	dY (MILS)
1	0	0	5	5
2	-7.25	0	5	5
3	-14.25	-7.09	5	5
4	-14.25	-14.4	5	5
5	-14.25	-21.7	5	5
6	-14.25	-28.9	5	5
7	-7.25	-36.2	5	5
8	0	-36.2	5	5
9	7.25	-36.2	5	5
10	14.5	-36.2	5	5
11	21.7	-28.9	5	5
12	21.7	-21.7	5	5
13	21.7	-14.4	5	5
14	21.7	-7.1	5	5
15	14.5	0	5	5
16	7.3	0	5	5

NOTE:

6. Coordinate Origin is Centroid of PAD 1

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
June 27, 2014	FN6475.4	Added “EH” finished good ISL73096EHVF, SL73096EHVX, ISL73127EHVF, ISL73127EHVX and ISL73128EHVFX to ordering information table. Added EH parts to title and mentioned throughout datasheet where applicable.
November 12, 2009	FN6475.3	Converted to new Intersil template. Changed App Note Reference from “AN9315” to “AN1503” to reflect new app note for the radiation hardened product. Updated ordering information with package column, notes to match lead finish and MSL note.
March 23, 2009	FN6475.2	Under Pinouts, changed DIP symbols to flatpack symbols. Changed (16 LD SBDIP) CDIP2-T16 to (16 LD Flatpack) CDFP4-F16. Under Ordering Information, added the following flatpack device types: 5962F0721801VXC (ISL73096RHVF), 5962F0721802VXC (ISL73127RHVF) and 5962F0721803VXC (ISL73128RHVF).
December 20, 2007	FN6475.1	Added ISL73127RH & ISL73128RH device types.
March 29, 2007	FN6475.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated data sheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

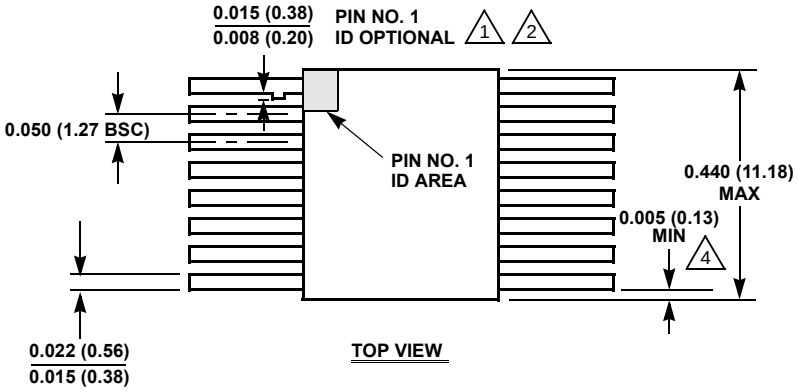
You may report errors or suggestions for improving this data sheet by visiting www.intersil.com/ask.

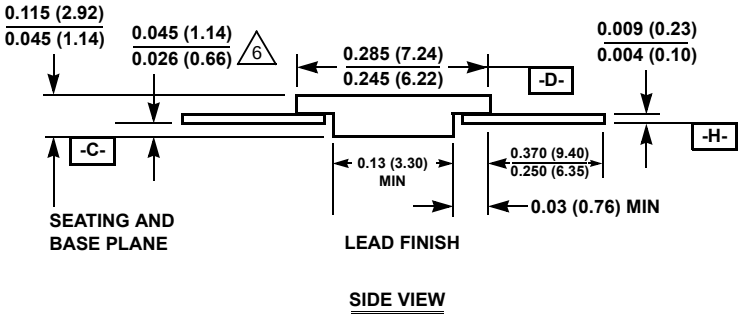
Reliability reports are also available from our website at www.intersil.com/support

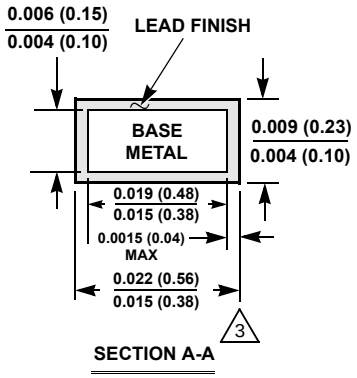
Package Outline Drawing

K16.A

16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 2, 1/10







NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.